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| U.S. Department of Commerce, Patent and Trademark Office | | | | Atty Docket No. | | Serial No. | |
| | | | | M-15206 US | | 10/629,221 | |
| INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) | | | | Applicant(s) | | | |
| | | | | Om P. Agrawal et al. | | | |
| | | | | Filing Date | | Group | |
| | | | | 07/29/2003 | | 2816 | |

| U.S. Patent Documents | | | | | | | |
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| *Examiner Initial | | Document Number | Date | Name | Class | Subclass | Filing Date If Appropriate |
| | AA | | | | | | |
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| Foreign Patent Documents | | | | | | | | |
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| | | Document | Date | Country | Class | Subclass | Translation | |
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| OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) | | |
|--|----|---|
| <i>Cse</i> | AQ | U.S. Patent Application No. 10/629,223 entitled "Clock Generator" filed on July 29, 2003 |
| <i>Cse</i> | AR | 3.3V Programmable Skew PLL Clock Driver Turboclock, IDT5V991A, Commercial and Industrial Temperature Ranges, September 2001 |
| <i>Cse</i> | AS | One-PLL General Purpose Flash-Programmable Clock Generator, CY22050, Cypress Semiconductor Corporation, San Jose, CA, Revised December 14, 2002 |

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| Examiner | <i>Cassandra Cop</i> | Date Considered | <i>7/8/04</i> |
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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| | AA | | | | | | |
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| Foreign Patent Documents | | | | | | | | |
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| OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.) | | |
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| CSL | AQ | ICS541, PLL Clock Divider, Revision 021303, Integrated Circuit Systems, Inc. |
| CSL | AR | User Programmable Laser Engine Pixel Clock Generator, ICS1574B, 08/31/2000 |
| CSL | AS | EEPROM Programmable 3-PLL Clock Generator IC, FS6370-01, AMI Semiconductor |

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| Examiner | Cassandra Coy | Date Considered | 7/13/04 |
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